CLAIM SET AS AMENDED

1. (currently amended) A method for estimating one of the frequency (f_{a1}) and the phase (ϕ_{a1}) of a digital input signal ($x(i)$) having the following process steps:

- determining phase values ($C_{a1}(i)$) of the digital input signal ($x(i)$),

- summing the phase values ($C_{a1}(i)$) over a predetermined summation length N/B which is a predetermined fraction 1/B of an observation length of N phase values ($C_{a1}(i)$), to create added-up phase values ($S_{a1}(i)$),

- reducing a sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with a sampling rate (f_{a2}) of the phase values ($C_{a1}(i)$),

- delaying the added-up phase values ($S_{a1}(i)$) with at least B-1 delay elements, each of which delays the added-up phase values ($S_{a1}(i)$) by one sampling period of the reduced sampling rate ($f_{a2}\bullet B/N$),

- adding up the delayed ~~differently delayed~~ added-up phase values ($S_{a1}(i)$) to create a resulting pulse response (h_f) of the frequency so that one of the resulting pulse responses (h_f) of the frequency (f_{a1}) is constant positive in a first interval [[(40)]], is zero in a second interval [[(41)]], and is constant negative in a third interval (42), and such that a [[the]] resulting pulse response

(h_ϕ) of the phase ~~that~~ is constant in at least a middle interval [[(43)]] of the observation length [[(N)]] and is otherwise zero.

2. (currently amended) The method of claim 1, wherein the fraction 1/B is 1/(3•n), where n is a positive [[an]] integer.

3. (currently amended) The method of claim 2, wherein the fraction 1/B is 1/3, wherein a first delay element and second delay element ~~two delay elements~~ ~~(15, 16)~~ are provided, and wherein the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element ~~(16)~~ is subtracted from the added-up phase value ($S_{a1}(i)$) at the input of the first delay element ~~(15)~~ to determine the estimated frequency (f_{a1}).

4. (currently amended) The method of claim 2, wherein the fraction 1/B is 1/3, wherein a first delay element and second delay element ~~two delay elements (15, 16)~~ are provided, and wherein the added-up phase value ($S_{a1}(i)$) at the input of the first delay element [[(15)]], the added-up phase value ($S_{a1}(i)$) at the output of the first delay element, [[(15)]] and the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] are summed to determine the estimated phase (ϕ_{a1}).

5. (currently amended) The method of claim 2 [[3]], wherein the

fraction 1/B is 1/6, wherein a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ are provided, and wherein the added-up phase value at the input of the first delay element [[(26)]] and the added-up phase value ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]] are added, and from this the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] and ($S_{a1}(i-5)$) at the output of the fifth delay element [[(30)]] are subtracted to determine the estimated frequency (f_{a1}).

6. (currently amended) The method of claim 2 [[4]], wherein the fraction 1/B is equal to 1/6, wherein a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ are provided, and the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], ($S_{a1}(i-2)$) at the output of the second delay element [[(27)], ($S_{a1}(i-3)$) at the output of the third delay element [[(28)]] and ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] are summed to determine the estimated phase (ϕ_{a1}).

7. (currently amended) The method of claim 1, wherein each of the first interval ~~intervals~~ [[(40)]], the second interval, [[(41)]] and the third interval [[(42)]] of the resulting pulse response (h_f) of the frequency has a length of N/B, in particular 1/3 N.

8. (currently amended) The method of claim 1, wherein the middle interval [[(43)]] of the resulting pulse response (h_ϕ) of the phase has the length N•(3n-n)/3•n, in particular 2/3 N, where n is a positive integer.

9. (currently amended) The method of claim 1, wherein the middle interval [[(43)]] of the resulting pulse response (h_ϕ) extends over the total observation length N.

10. (currently amended) An apparatus for estimating the frequency (f_{a1}) and/or the phase (ϕ_{a1}) of a digital input signal (x(i)), the apparatus comprising:

- a phase determining device, [[(3)]] which determines phase values (C_{a1}(i)) of the digital input signal (x(i)),
- a first filter [[(4)]], which adds up the phase values (C_{a1}(i)) over a predetermined summation length N/B, which is a predetermined fraction 1/B of an observation length of N phase values (C_{a1}(i)), to form added-up phase values (S_{a1}(i)), and the sampling rate of the added-up phase values (S_{a1}(i)) is reduced by a factor N/B in comparison with a sampling rate (f_{a2}) of the phase values (C_{a1}(i)),
- a second filter [[(8)]] which delays the added-up phase values (S_{a1}(i)) in a chain of at least B-1 delay elements ~~(15, 16; 26-30)~~, which respectively delay the added-up phase values (S_{a1}(i)) by one sampling period of the reduced sampling rate (f_{a2}•B/N), and adds or

subtracts the ~~differently delayed~~ delayed added-up phase values ($S_{a1}(i)$)[[,]] to create a resulting pulse response (h_f) of the frequency so that at least one of: a resulting pulse response (h_f) of the frequency is constant positive in a first interval [[(40)]], is zero in a second interval, or [[(41)]] ~~and~~ is constant negative in a third interval, ~~(42);~~ and wherein ~~they are added to create~~ a resulting pulse response (h_ϕ) of the phase is created so that the resulting pulse response (h_ϕ) of the phase is constant in at least a middle interval [[(43)]] and is otherwise zero.

11. (currently amended) The apparatus of claim 10, wherein the phase determination device [[(3)]] has a counter [[(24)]] whose count is read out at a constant sampling rate (f_{a2}).

12. (currently amended) The apparatus of claim 10, wherein the first filter [[(4)]] has an integrator [[(10)]], a differentiator [[(11)]] and a first sampling-rate converter [[(14)]] arranged between the integrator [[(10)]] and the differentiator [[(11)]] to reduce the sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with the sampling rate frequency (f_{a2}) of the phase values ($C_{a1}(i)$).

13. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/3, and the second filter [[(8)]] has a first

delay element and a second delay element ~~two delay elements (15, 16)~~ and a subtractor, [[(18)]] which subtracts the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] from the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(15)]] to determine the estimated frequency (f_{a1}).

14. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/3, and the second filter [[(8)]] has a first delay element and a second delay element ~~two delay elements (15, 16)~~ and adders ~~(20, 21)~~ which sum the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(15)]], the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element, [[(15)]] and the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] to determine the estimated phase (ϕ_{a1}).

15. (currently amended) The apparatus of claim 13, wherein a second sampling-rate converter ~~(37, 23)~~ is arranged to follow at least one of the adders ~~(20, 21)~~ and the subtractor [[(18)]] to reduce the sampling rate by a factor of 3.

16. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/6, and the second filter [[(8)]] has a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~, an

adder [[(31)]] that adds up the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(26)]] and the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], and subtractors ~~(32, 33)~~ which subtract therefrom the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] and the added-up phase values ($S_{a1}(i-5)$) at the output of the fifth delay element [[(30)]] to determine the estimated frequency (f_{a1}).

17. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/6, and the second filter [[(8)]] has a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ and adders ~~(34-36)~~ which add up the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(27)]], the added-up phase values ($S_{a1}(i-3)$) at the output of the third delay element [[(28)]] and the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] to determine the estimated phase (ϕ_{a1}).

18. (currently amended) The apparatus of claim 16, wherein a second sampling-rate converter ~~(37, 23)~~ is respectively arranged after at least one of the adders ~~(34, 36)~~ and the subtractors ~~(32, 33)~~ for reducing the sampling rate by a factor of 6.